Data Sheet For Video DeInterlacer

DOCUMENT REVISION HISTORY

Revision	Date	Change Description	Author
1.0	16th Dec '11	Initial Version	KT
REL 1.0	16th Aug '12	Removed implementation results	VC

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1 Introduction

1.1 Purpose

This document describes the Technical Specification of the Video DeInterlacer core. It includes the overall architectural description, detailed functional specifications and interface definitions.

1.2 Features

The following lists the main features of the Video DeInterlacer Core:

- Weave Method of Video de-interlacing is supported
- Supports PAL or NTSC video mode
- RAM like memory interface with separate read and write controls
- Fully stallable interfaces on both input and output

1.3 Acronyms and Abbreviations

Table 1: Acronyms & Abbreviations

Term	Meaning
FPGA	Field Programmable Gate Array
NTSC	National Television Standards Committee
PAL	Phase Alternating Line
RAM	Random Access Memory

2 Video DeInterlacer

2.1 Block Diagram

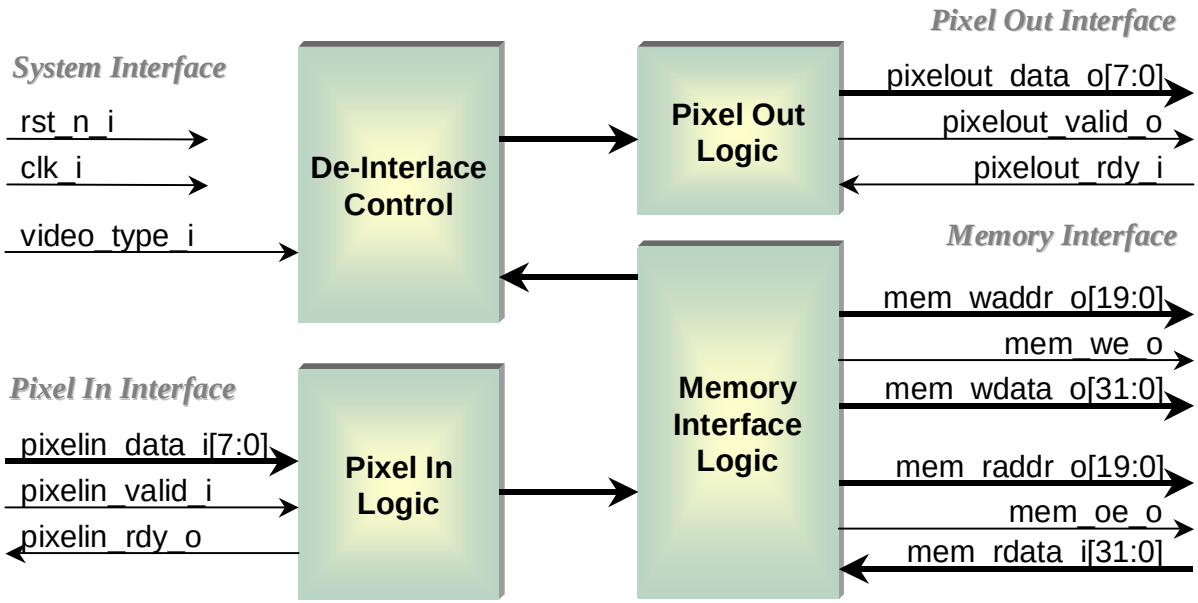

Figure 1: Video De-Interlacer Block Diagram

2.2 Description

The main blocks in Video DeInterlacer are:

- **Pixel In Logic**: This interface accepts the interlaced video pixel input data and the valid signal whenever the core is ready to accept new data and converts the data into 32bit data which can be fed to memory interface logic.
- **Pixel Out Logic**: This interface accepts the deinterlaced 32bit video data from the Deinterlace Control module and generates 8bit video pixel output and valid signal on the Pixel Out interface whenever ready input is asserted at this interface.
- **De-Interlace Control**: This logic takes care of video deinterlacing using the weave method. This module takes care of buffer handling and address generation for memory read. Such that a weaved output is generated from the input odd and even fields.
- **Memory Interface Logic**: Here the read and write control signals, the address generation is taken care that is routed to the appropriate read and write ports of the Memory Interface

2.3 I/O Signal Description

Table 2: Video DeInterlacer IO Signal Description

Signal	I/O	Width	Description
RST_N_I	I	1	Active low Asynchronous reset input.
CLK_I	I	1	Clock input to the core. This clock determines the operating frequency of the core. The memory read/write operations also takes place wrt this clock
VIDEO_TYPE_I	I	1	Video type select input. This input selects the operating mode of the core. 0 – PAL 1 – NTSC
PIXELIN_DATA_I	I	8	PixelIn Interface data input. This is the interlaced video input to the core. And the input is valid when PIXELIN_VALID_I is asserted.
PIXELIN_VALID_I	I	1	PixelIn Interface data valid input. This input qualifies the PIXELIN_DATA_I data.
PIXELIN_RDY_O	O	1	PixelIn Interface data ready output. This signal indicates the ability of core to accept data input at the PixelIn Interface.
PIXELOUT_DATA_O	O	8	PixelOut Interface data output. This is the DeInterlaced video output generated by the core. And the output is valid when PIXELOUT_VALID_O is asserted.
PIXELOUT_VALID_O	O	1	PixelOut Interface data valid output. This signal validates the DeInterlaced video output PIXELOUT_DATA_O generated by the core.
PIXELOUT_RDY_I	I	1	PixelOut Interface data ready input. This signal enables the core to output new data on PIXELOUT_DATA_O.
MEM_WADDR_O	O	20	Memory write address output. This is the address for the RAM write interface.
MEM_WE_O	O	1	Memory write enable output. This is the enable signal for the RAM write interface.
MEM_WDATA_O	O	32	Memory write data output. This is the data bus for the RAM write interface.

Signal	I/O	Width	Description
MEM_RADDR_O	O	20	Memory read address output. This is the address for the RAM read interface.
MEM_OE_O	O	1	Memory read enable output. This is the enable signal for the RAM read interface.
MEM_RDATA_I	I	32	Memory read data output. This is the data bus for the RAM read interface.

3 Timing Waveforms

3.1 PixelIn Interface

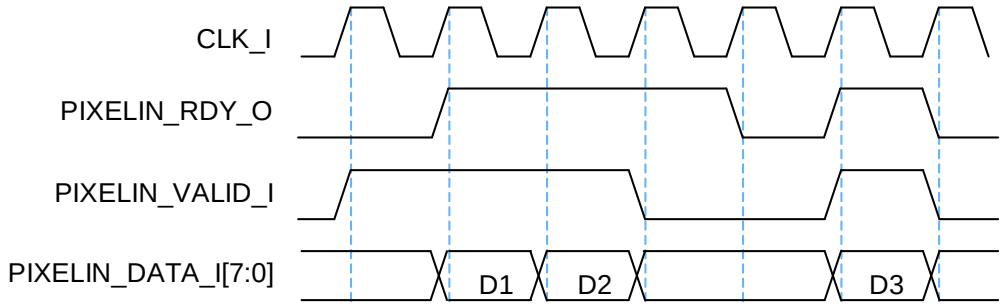

Figure 2: PixelIn Interface Timing Diagram

3.2 PixelOut Interface

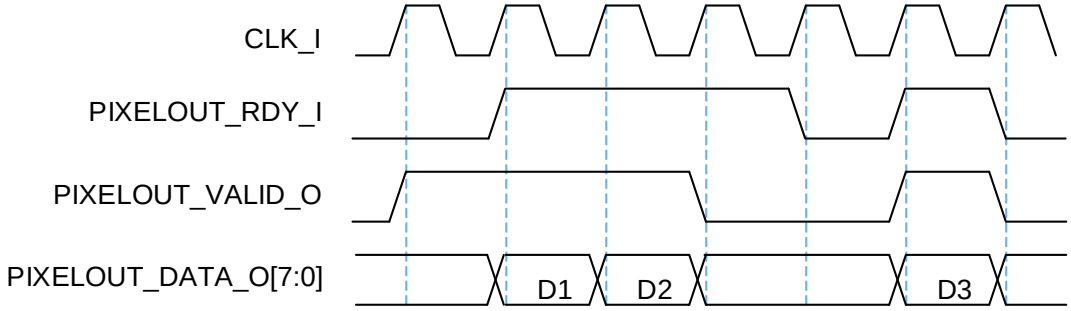

Figure 3: PixelOut Interface Timing Diagram

3.3 Memory Interface

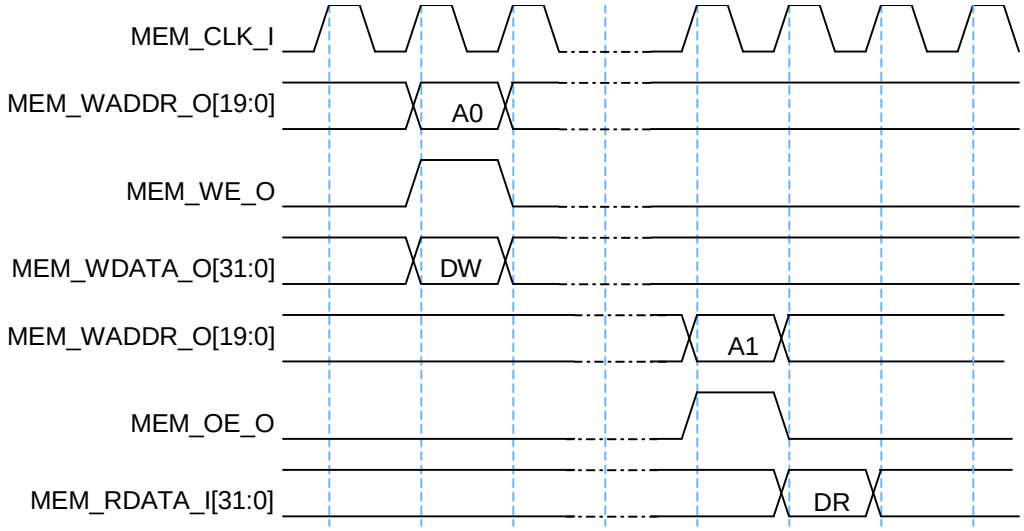

Figure 4: Memory Interface Timing Diagram